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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/730,780	PORTERFIELD, A. KENT	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38 and 40-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38 and 40-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 27th of December 2004. Claims 1-10, 19-22, 24, 34, 36, 37, 40, 42, 51, 55 and 56 have been amended; claims 39 and 57-60 have been canceled; and no claim has been newly added since the RCE Non-Final Office Action was mailed on 24th of August 2004. Currently, claims 1-38 and 40-56 are pending in this application.

Claim Objections

2. Claim 5 is objected to because of the following informalities:

Substitute "a internal status information" by --an internal status information-- in line 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 2, 16-20, 34, 35, 38, 40, 51, 52, 55 and 56 are rejected under 35 U.S.C. 102(e) as being anticipated by Ajanovic et al. [US 6,516,375 B1; hereinafter Ajanovic].

Referring to claim 1, Ajanovic discloses a bus arbitration method (See Fig. 2 and col. 3, line 65 through col. 4, line 26) for a processor based system (i.e., system 100 of Fig. 1; See Fig. 1 and col. 2, lines 50-60), said system comprising a link bus (i.e., memory control hub agent MCH 120, input/output control hub agent ICH 140, and hub interfaces A, C, D in Fig. 1), said link bus comprising a link bus hub (i.e., MCH 120 and ICH 140 in Fig. 1) and a plurality of link bus segments (i.e., HI A, HI C and HI D in Fig. 1), each link bus segment comprising a plurality of lines (See Fig. 14, and Table 3 on col. 10-11) for communicating commands, addresses, data (i.e., communicating commands, addresses, data via PD[15:0] being comprised of a plurality of lines), and a single-bit link status signal (i.e., a single bit status signal on a line of RQA or RQB in Fig, 14), each link bus segment coupled to said link bus hub (i.e., HI A, HI C

and HI D coupled to said link bus hub, which is MCH 120 and ICH 140 in Fig. 1) and one respective satellite device (i.e., HI A coupled to Bridge 127, HI C coupled to Network Interface 143, and HI D coupled to Fiber Channel 145 in Fig. 1) to form a point-to-point link between said link bus hub and respective satellite device (i.e., HI A, HI C and HI D coupled to said link bus hub, which is MCH and ICH, forming said point-to-point link), one of said respective satellite device being a first device (i.e., a bus agent, e.g., one of Bridge 127, Network Interface 143, and Fiber Channel 145 in Fig. 1), a processor coupled to said hub device (i.e., said link bus hub, which is MCH 120 and ICH 140, coupled to processors 102, 104, 106 and 108 in Fig. 1) via a processor bus (i.e., processor bus 110 of Fig. 1) and a memory device (i.e., main memory 123 of Fig. 1) coupled to said link bus hub (i.e., said link bus hub, which is MCH 120 and ICH 140, coupled to main memory 123 in Fig. 1) by a memory bus (i.e., bus between memory interface 122 and main memory 123 in Fig. 1), said method comprising the steps of issuing, from one of said first device and said hub device (i.e., from one of said bus agents), an arbitration request (i.e., ARBITRATION 202 and REQUEST 204 in Fig. 2) on a portion of said plurality of lines (i.e., a RQA line or a RQB line of a plurality lines between Agent A 1410 and Agent B 1420 in Fig. 14) associated with said single-bit link status signal (i.e., a RQA line being associated with a single bit status signal from Agent A to Agent B, and a RQB line being associated with a single bit status signal from Agent B to Agent A in Fig, 14) of said link bus (See col. 4, lines 1-6); determining, at said first device and said hub device, whether control of said link bus can be transferred from a bus master (i.e., hub agent A in Fig. 13) to said device (i.e., hub agent B in Fig. 13) issuing said arbitration request (i.e., requesting ownership of hub interface; See col. 9, lines 48-50); and if it is determined that control of said link bus can be transferred (See col. 9, lines 52-54), transferring control of said link bus from said bus master to said device issuing said arbitration request (i.e., releasing hub agent A's ownership; See step 1310 in Fig. 13 and col. 9, lines 60-61), wherein control of said link bus is granted by said first device and said hub device (See Figs. 11-13; i.e., wherein in fact that hub agent A releases hub interface to hub agent B in Fig.

13, step 1310, inherently anticipates that control of link bus is granted by said first device and said hub device).

Referring to claim 2, Ajanovic teaches inspecting (i.e., sampling) an internal arbitration state (i.e., state of hub agent) and an internal status information (i.e., active or inactive; See Fig. 11 and col. 9, lines 12-16); and determining if control of said link bus can be transferred (See col. 9, lines 48-50) based on said inspected (i.e., sampled) internal arbitration state and said inspected internal status information (See Figs. 11 and 12; i.e., based on state of hub agent if it is active or inactive; See col. 9, lines 12-16 and 34-38).

Referring to claims 16 and 17, Ajanovic teaches said link bus (i.e., memory control hub agent MCH 120, input/output control hub agent ICH 140, and hub interfaces A, C, D in Fig. 1) comprising a link bus status line (i.e., RQA and RQB in Fig. 14) and said issuing step comprising propagating a signal (i.e., transmitting active or inactive signal; See col. 9, lines 12-16 and 34-38) on said link bus status line in time-multiplexing (See col. 8, line 56 through col. 9, line 4).

Referring to claim 18, Ajanovic teaches said issuing step through said transferring step are performed in accordance with a link bus protocol (i.e., PROTOCOL LAYER) of said link bus (See col. 5, line 65 through col. 6, line 23).

Referring to claim 19, Ajanovic discloses a method of arbitrating control (See Fig. 2 and col. 3, line 65 through col. 4, line 26) of a link bus (i.e., memory control hub agent MCH 120, input/output control hub agent ICH 140, and hub interfaces A, C, D in Fig. 1) of a computer system (i.e., system 100 of Fig. 1; See Fig. 1 and col. 2, lines 50-60), said link bus comprising a link bus hub (i.e., MCH 120 and ICH 140 in Fig. 1) and a plurality of link bus segments (i.e., HI A, HI C and HI D in Fig. 1), each link bus segment comprising a plurality of lines (See Fig. 14, and Table 3 on col. 10-11) for communicating commands, addresses, data (i.e., communicating commands, addresses, data via PD[15:0] being comprised of a plurality of lines), and a single-bit link status signal (i.e., a single bit status signal on a line

of RQA or RQB in Fig, 14), each link bus segment coupled to said link bus hub (i.e., HI A, HI C and HI D coupled to said link bus hub, which is MCH 120 and ICH 140 in Fig. 1) and one respective satellite device (i.e., HI A coupled to Bridge 127, HI C coupled to Network Interface 143, and HI D coupled to Fiber Channel 145 in Fig. 1) to form a point-to-point link between said link bus hub and respective satellite device (i.e., HI A, HI C and HI D coupled to said link bus hub, which is MCH and ICH, forming said point-to-point link), said hub device coupled to a processor (i.e., said link bus hub, which is MCH 120 and ICH 140, coupled to processors 102, 104, 106 and 108 in Fig. 1) of said computer system (i.e., system 100 of Fig. 1) by a processor bus (i.e., processor bus 110 of Fig. 1) and coupled to a memory device (i.e., main memory 123 of Fig. 1) of said computer system (i.e., system 100 of Fig. 1) by a memory bus (i.e., bus between memory interface 122 and main memory 123 in Fig. 1), said link bus being a source strobed bus (i.e., hub interface with source synchronous clock mode; See col. 4, lines 35-38 and col. 6, lines 24-36), said method comprising the steps of: time-multiplexing, from one of said satellite device and said hub device (See col. 8, line 56 through col. 9, line 4), an arbitration request signal on said single-bit link status line (i.e., a RQA line being associated with a single bit status signal from Agent A to Agent B, and a RQB line being associated with a single bit status signal from Agent B to Agent A in Fig, 14); detecting (i.e., sampling), at the other of said satellite device and said hub device, said arbitration request signal (See col. 9, lines 12-16 and 34-38); determining, at said satellite device and said hub device, whether control of the link bus can be transferred from a bus master (i.e., hub agent A in Fig. 13) to said device (i.e., hub agent B in Fig. 13) issuing said arbitration request (i.e., requesting ownership of hub interface; See col. 9, lines 48-50); and if it is determined that control of said link bus can be transferred (See col. 9, lines 52-54), transferring control of said link bus from said bus master to said device issuing said arbitration request (i.e., releasing hub agent A's ownership; See step 1310 in Fig. 13 and col. 9, lines 60-61), wherein control of said link bus is granted by said first device and said hub device (See Figs. 11-13; i.e., wherein in fact that hub agent A releases hub interface to hub agent B in Fig.

13, step 1310, inherently anticipates that control of link bus is granted by said first device and said hub device).

Referring to Claim 20, Ajanovic teaches inspecting (i.e., sampling) an internal arbitration state (i.e., state of hub agent) and a status information (i.e., active or inactive; See Fig. 11 and col. 9, lines 12-16) contained on each of said satellite device and said hub device (See Fig. 14 and col. 10, lines 24+); and determining if control of said link bus can be transferred (See col. 9, lines 48-50) based on said inspected (i.e., sampled) internal arbitration state and status information (See Figs. 11 and 12; i.e., based on state of hub agent if it is active or inactive; See col. 9, lines 12-16 and 34-38).

Referring to claim 34, Ajanovic discloses a processor system (i.e., system 100 of Fig. 1; See Fig. 1 and col. 2, lines 50-60) comprising: a processor (i.e., processors 102, 104, 106 and 108 in Fig. 1); a link bus (i.e., memory control hub agent MCH 120, input/output control hub agent ICH 140, and hub interfaces A, C, D in Fig. 1), said link bus comprising a link bus hub (i.e., MCH 120 and ICH 140 in Fig. 1) and a plurality of link bus segments (i.e., HI A, HI C and HI D in Fig. 1), each link bus segment comprising a plurality of lines (See Fig. 14, and Table 3 on col. 10-11) for communicating commands, addresses, data (i.e., communicating commands, addresses, data via PD[15:0] being comprised of a plurality of lines), and a single-bit link status signal (i.e., a single bit status signal on a line of RQA or RQB in Fig, 14), each link bus segment coupled to said link bus hub (i.e., HI A, HI C and HI D coupled to said link bus hub, which is MCH 120 and ICH 140 in Fig. 1) and one respective satellite device (i.e., HI A coupled to Bridge 127, HI C coupled to Network Interface 143, and HI D coupled to Fiber Channel 145 in Fig. 1) to form a point-to-point link between said link bus hub and respective satellite device (i.e., HI A, HI C and HI D coupled to said link bus hub, which is MCH and ICH, forming said point-to-point link), one of said respective satellite device being a first device (i.e., a bus agent, e.g., one of Bridge 127, Network Interface 143, and Fiber Channel 145 in Fig. 1), said link bus hub being coupled to said processor (i.e., said link bus hub, which is MCH 120 and ICH 140, coupled to processors 102, 104, 106

and 108 in Fig. 1) via a processor bus (i.e., processor bus 110 of Fig. 1); wherein said first device and said link hub arbitrate a control of link bus (See Fig. 2 and col. 3, line 65 through col. 4, line 26) by issuing, from one of said satellite device and said link hub (i.e., from one of said bus agents), an arbitration request (i.e., ARBITRATION 202 and REQUEST 204 in Fig. 2) on a portion of said plurality of lines (i.e., a RQA line or a RQB line of a plurality lines between Agent A 1410 and Agent B 1420 in Fig. 14) associated with said single-bit link status signal (i.e., a RQA line being associated with a single bit status signal from Agent A to Agent B, and a RQB line being associated with a single bit status signal from Agent B to Agent A in Fig, 14) of said link bus (See col. 4, lines 1-6); determining, at said satellite device and said link hub, whether control of said link bus can be transferred from a bus master (i.e., hub agent A in Fig. 13) to said device (i.e., hub agent B in Fig. 13) issuing said arbitration request (i.e., requesting ownership of hub interface; See col. 9, lines 48-50); and transferring control of said link bus from said bus master to said device issuing said arbitration request (i.e., releasing hub agent A's ownership; See step 1310 in Fig. 13 and col. 9, lines 60-61).

Referring to claim 35, Ajanovic teaches said satellite device and said link hub determine if control of said link bus should be transferred by inspecting (i.e., sampling) respective internal arbitration state (i.e., state of hub agent) and status information (i.e., active or inactive; See Fig. 11 and col. 9, lines 12-16); and determining if control of said link bus can be transferred (See col. 9, lines 48-50) based on said inspected (i.e., sampled) internal arbitration state and status information (See Figs. 11 and 12; i.e., based on state of hub agent if it is active or inactive; See col. 9, lines 12-16 and 34-38).

Referring to claim 38, Ajanovic teaches said link bus (i.e., hub interfaces A, B, C and D in Fig. 1) is a source strobed bus (i.e., hub interface with source synchronous clock mode; See col. 4, lines 35-38 and col. 6, lines 24-36).

Referring to claim 40, Ajanovic teaches said arbitration request (i.e., ARBITRATION 202 and REQUEST 204 in Fig. 2) is issued by time-multiplexing an arbitration request signal (i.e., transmitting

active or inactive signal; See col. 9, lines 12-16 and 34-38) on said portion of said link bus associated with said single bit link status signal (i.e., on RQA or RQB signal line; See col. 8, line 56 through col. 9, line 4).

Referring to claim 51, Ajanovic discloses a processor based system (i.e., system 100 of Fig. 1; See Fig. 1 and col. 2, lines 50-60) comprising: a processor (i.e., processors 102, 104, 106 and 108 in Fig. 1); a link bus (i.e., memory control hub agent MCH 120, input/output control hub agent ICH 140, and hub interfaces A, C, D in Fig. 1), said link bus comprising a link bus hub (i.e., MCH 120 and ICH 140 in Fig. 1) and a plurality of link bus segments (i.e., HI A, HI C and HI D in Fig. 1), each link bus segment comprising a plurality of lines (See Fig. 14, and Table 3 on col. 10-11) for communicating commands, addresses, data (i.e., communicating commands, addresses, data via PD[15:0] being comprised of a plurality of lines), and a single-bit link status signal (i.e., a single bit status signal on a line of RQA or RQB in Fig, 14), each link bus segment coupled to said link bus hub (i.e., HI A, HI C and HI D coupled to said link bus hub, which is MCH 120 and ICH 140 in Fig. 1) and one respective satellite device (i.e., HI A coupled to Bridge 127, HI C coupled to Network Interface 143, and HI D coupled to Fiber Channel 145 in Fig. 1) to form a point-to-point link between said link bus hub and respective satellite device (i.e., HI A, HI C and HI D coupled to said link bus hub, which is MCH and ICH, forming said point-to-point link), one of said respective satellite device being a first device (i.e., a bus agent, e.g., one of Bridge 127, Network Interface 143, and Fiber Channel 145 in Fig. 1), said link bus hub being coupled to said processor (i.e., said link bus hub, which is MCH 120 and ICH 140, coupled to processors 102, 104, 106 and 108 in Fig. 1) via a first bus (i.e., processor bus 110 of Fig. 1); wherein said first device multiplexes (i.e., time-multiplexing in time slice; See col. 8, line 56 through col. 9, line 4) an arbitration signal (i.e., RQA/RQB's active/inactive signal shown in Figs. 11 and 12) on a portion of said lines (i.e., a RQA line and a RQB line of a plurality lines between Agent A 1410 and Agent B 1420 in Fig. 14) associated with said single-bit link bus status signal (i.e., a RQA signal being associated with a single bit status signal

from Agent A to Agent B, and a RQB signal being associated with a single bit status signal from Agent B to Agent A in Fig, 14; See col. 4, lines 1-6) in accordance with a link bus protocol (See col. 5, line 65 through col. 6, line 23) to become a master of said link bus (i.e., having ownership) during transmissions to said link hub (See col. 8, lines 43-55), and said link bus hub multiplexes another arbitration signal on said on said portion of said lines (i.e., a RQA line and a RQB line of a plurality lines between Agent A 1410 and Agent B 1420 in Fig. 14) associated with said single-bit link bus status signal (i.e., a RQA signal being associated with a single bit status signal from Agent A to Agent B, and a RQB signal being associated with a single bit status signal from Agent B to Agent A in Fig, 14; See col. 4, lines 1-6) in accordance with said link bus protocol to become a master of said link bus during transmissions to said first device (See Step 1310 in Fig. 13, and col. 8, line 56 through col. 9, line 4 and col. 9, lines 60-61; i.e., releasing hub agent A's ownership for hub agent B).

Referring to claim 52, Ajanovic teaches said link bus is a source strobed bus (i.e., hub interface with source synchronous clock mode; See col. 4, lines 35-38 and col. 6, lines 24-36).

Referring to claim 55, Ajanovic teaches said arbitration signals (i.e., RQA/RQB's active/inactive signals shown in Figs. 11 and 12) are time multiplexed on said portion of said lines (i.e., a RQA line and a RQB line of a plurality lines between Agent A 1410 and Agent B 1420 in Fig. 14) associated with said single-bit link bus status signal (i.e., a RQA signal being associated with a single bit status signal from Agent A to Agent B, and a RQB signal being associated with a single bit status signal from Agent B to Agent A in Fig, 14; See col. 4, lines 1-6) during a predetermined time window (i.e., time allotted to hub interface, viz., predetermined time slice; See col. 8, line 56 through col. 9, line 4).

Referring to claim 56, Ajanovic teaches said portion of said lines (i.e., a RQA line and a RQB line of a plurality lines between Agent A 1410 and Agent B 1420 in Fig. 14) associated with said single-bit link bus status signal (i.e., a RQA signal being associated with a single bit status signal from Agent A to Agent B, and a RQB signal being associated with a single bit status signal from Agent B to Agent A in

Fig, 14; See col. 4, lines 1-6) is used to transmit status information (i.e., active or inactive; See Fig. 11 and col. 9, lines 12-16) between said link hub (i.e., MCH 120 and ICH 140 in Fig. 1) and said satellite device (e.g., bus agents Bridge 127 in Fig. 1).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 3-15, 21-33, 36, 37 and 41-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic [US 6,516,375 B1] as applied to claims 1, 2, 16-20, 34, 35, 38, 40, 51, 52, 55 and 56 above, and further in view of Frame et al. [US 5,349,690 A; hereinafter Frame].

Referring to claim 3, Ajanovic discloses all the limitations of the claim 3, except that does not expressly teach said internal arbitration state comprising a current arbitration state selected from one of a park state indicating that there are no requests on said link bus, a grant-self state indicating that a device in control of said link bus is transferring information on said link bus, and a grant-other state indicating that another device is in control of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal arbitration state comprises a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in Fig. 2) indicating that there are no requests on a link bus (See col. 3, lines 28-31), a grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) indicating that a device (i.e., node) in control of said link bus is transferring information on said link bus, and a grant-other state (i.e., wait phase 48 in Fig. 2) indicating that another device is in control of said link bus (i.e., the current node loses the control of the bus, the another node wins the control of the bus; See col. 2, lines 45-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes)

connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 4, Ajanovic discloses all the limitations of the claim 4, except that does not expressly teach said internal status information comprising a current status value selected from one of a bus master arbitration request, a bus master transfer in progress, a bus slave arbitration request, and a bus slave transfer in progress.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (i.e., arbitration request at t_2 after transfer completion at t_1; See col. 3, lines 45-47), a bus master transfer in progress (i.e., reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1; See col. 3, lines 54-66), a bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes 12 and 16 in Fig. 1 via enabled path 42 of Fig. 2; See col. 3, lines 36-53), and a bus slave transfer in progress (i.e., selected arbitration request at t_1 and transfer phase at t_1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 5, Ajanovic discloses all the limitations of the claim 5, except that does not expressly teach said transferring step comprising modifying an internal arbitration state and an internal status information to reflect that said issuing device is a master of said link bus and that the other device connected to said link bus is a slave of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein a transferring step comprising modifying an internal arbitration state and an internal status information (i.e., modifying arbitration

phases, such that wait phase 48, selection phases 50, transfer phase 52, etc in Fig. 2) to reflect that said issuing device is a master of said link bus (i.e., winning node to control the bus) and that the other device connected to said link bus is a slave of said link bus (i.e., losing node not to control the bus; See col. 3, lines 21+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 6, Frame teaches said internal arbitration state information comprising a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in Fig. 2) indicating that there are no requests on said link bus (See col. 3, lines 28-31), a grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) indicating that a device (i.e., node) in control of said link bus is transferring information on said link bus, and a grant-other state (i.e., wait phase 48 in Fig. 2) indicating that another device is in control of said link bus (i.e., the current node loses the control of the bus, the another node wins the control of the bus; See col. 2, lines 45-68).

Referring to claim 7, Frame teaches said modifying step comprising at said first device (i.e., node 12 in Fig. 1), changing said internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said link bus hub (i.e., node 16 in Fig. 1), changing said internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 8, Frame teaches said modifying step comprising at said link bus hub (i.e., node 16 in Fig. 1), changing said internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said first device (i.e., node 12 in Fig. 1), changing said internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 9, Frame teaches said modifying step comprising at said first device (i.e., node 12 in Fig. 1), changing said internal arbitration state from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said link bus hub (i.e., node 16 in Fig. 1), changing said internal arbitration state from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 10, Frame teaches said internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (e.g., arbitration request from enabled message node 14 and 16 in Fig. 1 via enabled path 42 of Fig. 2, i.e., enabled arbitration status; See col. 3, lines 1-3), a bus master transfer in progress (i.e., transfer phase 52 after the node is selected as an arbitration winner), a bus slave arbitration request (e.g., path 44 of Fig. 2 for disabled message node 12 in Fig. 1, i.e., disabled arbitration status; See col. 3, lines 5-8), and a bus slave transfer in progress (i.e., wait phase 48 after the node is lost the bus control; a data transfer on the bus is controlled by another node).

Referring to claim 11, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus master arbitration request (i.e., an arbitration request at t_2 after transfer completion at t_1) and not said bus slave arbitration request (i.e., not an arbitration request at t_1 from enabled message nodes). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said park state to said grant-other state if said internal status reflects said bus master arbitration request and not said bus slave arbitration request.

Referring to claim 12, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in

Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes, and the highest priority node wins to control the bus; See col. 3, lines 42-45).

Referring to claim 13, Frame teaches said internal arbitration state is changed from said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes) and not said bus slave transfer in progress state (i.e., after completion the bus slave transfer in progress state, caused by a selected arbitration request at t_1 and transfer phase at t_1). Refer to col. 3, lines 45-47.

Referring to claim 14, Frame teaches said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., an arbitration request at t_1 from enabled message nodes, which has been waiting in wait phase 48 in Fig. 2) and not said bus master transfer in progress state (i.e., after completion the transfer phase at t_2, caused by a reselected arbitration request at t_2 after transfer completion at t_1). See Fig. 2 and col. 3, lines 21+ for the operation of the fair arbitration scheme.

Referring to claim 15, Frame teaches said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said park state (i.e., bus idle state 40 in Fig. 2) if said internal status does not reflect said bus master arbitration request (i.e., no arbitration request at t_2 after transfer completion at t_1), said bus slave arbitration request (i.e., no arbitration request at t_1 from enabled message nodes) and said bus master transfer in progress state (i.e., no reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if said

internal status does not reflect said bus master arbitration request, said bus slave arbitration request and said bus master transfer in progress state, i.e., said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if the bus is not busy.

Referring to claim 21, Ajanovic discloses all the limitations of the claim 21, except that does not expressly teach said internal arbitration state information comprising a current arbitration state selected from one of a park state indicating that there are no requests on said link bus, a grant-self state indicating that a device in control of said link bus is transferring information on said link bus, and a grant-other state indicating that another device is in control of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal arbitration state information comprises a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in Fig. 2) indicating that there are no requests on said link bus (See col. 3, lines 28-31), a grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) indicating that a device (i.e., node) in control of said link bus is transferring information on said link bus, and a grant-other state (i.e., wait phase 48 in Fig. 2) indicating that another device is in control of said link bus (i.e., the current node loses the control of the bus, the another node wins the control of the bus; See col. 2, lines 45-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 22, Ajanovic discloses all the limitations of the claim 22, except that does not expressly teach said internal status information comprising a current status value selected from one of a bus master arbitration request, a bus master transfer in progress, a bus slave arbitration request, and a bus slave transfer in progress.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (i.e., arbitration request at t_2 after transfer completion at t_1; See col. 3, lines 45-47), a bus master transfer in progress (i.e., reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1; See col. 3, lines 54-66), a bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes 12 and 16 in Fig. 1 via enabled path 42 of Fig. 2; See col. 3, lines 36-53), and a bus slave transfer in progress (i.e., selected arbitration request at t_1 and transfer phase at t_1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 23, Ajanovic discloses all the limitations of the claim 23, except that does not expressly teach said transferring step comprising modifying internal arbitration state and status information on each of said satellite device and said hub device to reflect that said issuing device is a master of said link bus and that the other device connected to said link bus is a slave of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein an transferring step comprising modifying internal arbitration state and status information (i.e., modifying arbitration phases, such that wait phase 48, selection phases 50, transfer phase 52, etc in Fig. 2) on each of said satellite device (e.g., node 12 in Fig. 1) and said hub device (e.g., node 16 in Fig. 1) to reflect that said issuing device is a master of said link bus (i.e., winning node to control the bus) and that the other device connected to said link bus is a slave of said link bus (i.e., losing node not to control the bus; See col. 3, lines 21+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said

bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 24, Frame teaches said internal arbitration state information comprising a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in Fig. 2), a grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) and a grant-other state (i.e., wait phase 48 in Fig. 2).

Referring to claim 25, Frame teaches said modifying step comprising at said satellite device (i.e., node 12 in Fig. 1), changing said internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 26, Frame teaches said modifying step comprising at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said satellite device (i.e., node 12 in Fig. 1), changing said internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 27, Frame teaches said modifying step comprising at said satellite device (i.e., node 12 in Fig. 1), changing said internal arbitration state from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 28, Frame teaches said internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (e.g., arbitration request from enabled message node 14 and 16 in Fig. 1 via enabled path 42 of Fig. 2, i.e., enabled arbitration status; See col. 3, lines 1-3), a bus master transfer in progress (i.e., transfer phase 52 after the

node is selected as an arbitration winner), a bus slave arbitration request (e.g., path 44 of Fig. 2 for disabled message node 12 in Fig. 1, i.e., disabled arbitration status; See col. 3, lines 5-8), and a bus slave transfer in progress (i.e., wait phase 48 after the node is lost the bus control; a data transfer on the bus is controlled by another node).

Referring to claim 29, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus master arbitration request (i.e., an arbitration request at t_2 after transfer completion at t_1) and not said bus slave arbitration request (i.e., not an arbitration request at t_1 from enabled message nodes). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said park state to said grant-other state if said internal status reflects said bus master arbitration request and not said bus slave arbitration request.

Referring to claim 30, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes, and the highest priority node wins to control the bus; See col. 3, lines 42-45).

Referring to claim 31, Frame teaches said internal arbitration state is changed from said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes) and not said bus slave transfer in progress state (i.e., after completion the bus slave transfer in progress state, caused by a selected arbitration request at t_1 and transfer phase at t_1). Refer to col. 3, lines 45-47.

Referring to claim 32, Frame teaches said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase

52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., an arbitration request at t_1 from enabled message nodes, which has been waiting in wait phase 48 in Fig. 2) and not said bus master transfer in progress state (i.e., after completion the transfer phase at t_2, caused by a reselected arbitration request at t_2 after transfer completion at t_1). See Fig. 2 and col. 3, lines 21+ for the operation of the fair arbitration scheme.

Referring to claim 33, Frame teaches said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said park state (i.e., bus idle state 40 in Fig. 2) if said internal status does not reflect said bus master arbitration request (i.e., no arbitration request at t_2 after transfer completion at t_1), said bus slave arbitration request (i.e., no arbitration request at t_1 from enabled message nodes) and said bus master transfer in progress state (i.e., no reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if said internal status does not reflect said bus master arbitration request, said bus slave arbitration request and said bus master transfer in progress state, i.e., said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if the bus is not busy.

Referring to claim 36, Ajanovic discloses all the limitations of the claim 36, except that does not expressly teach said internal arbitration state information comprising a current arbitration state selected from one of a park state indicating that there are no requests on said link bus, a grant-self state indicating that a device in control of said link bus is transferring information on said link bus, and a grant-other state indicating that another device is in control of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal arbitration state comprises a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in

Fig. 2) indicating that there are no requests on a link bus (See col. 3, lines 28-31), a grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) indicating that a device (i.e., node) in control of said link bus is transferring information on said link bus, and a grant-other state (i.e., wait phase 48 in Fig. 2) indicating that another device is in control of said link bus (i.e., the current node loses the control of the bus, the another node wins the control of the bus; See col. 2, lines 45-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 37, Ajanovic discloses all the limitations of the claim 37, except that does not expressly teach said internal status information comprising a current status value selected from one of a bus master arbitration request, a bus master transfer in progress, a bus slave arbitration request, and a bus slave transfer in progress.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (i.e., arbitration request at t_2 after transfer completion at t_1; See col. 3, lines 45-47), a bus master transfer in progress (i.e., reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1; See col. 3, lines 54-66), a bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes 12 and 16 in Fig. 1 via enabled path 42 of Fig. 2; See col. 3, lines 36-53), and a bus slave transfer in progress (i.e., selected arbitration request at t_1 and transfer phase at t_1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes)

connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 41, Ajanovic discloses all the limitations of the claim 41, except that does not expressly teach said satellite device and said link hub transfer control of said link bus by modifying respective internal arbitration state and status information to reflect that said issuing device is a master of said link bus and that the other device connected to said link bus is a slave of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein a satellite device (e.g., node 12 in Fig. 1) and a link hub (e.g., node 16 in Fig. 1) transfer control of a link bus (i.e., bus 10 of Fig. 1) by modifying an internal arbitration state and an internal status information (i.e., modifying arbitration phases, such that wait phase 48, selection phases 50, transfer phase 52, etc in Fig. 2) to reflect that said issuing device is a master of said link bus (i.e., winning node to control the bus) and that the other device connected to said link bus is a slave of said link bus (i.e., losing node not to control the bus; See col. 3, lines 21+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 42, Frame teaches said internal arbitration state information comprising a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in Fig. 2) indicating that there are no requests on said link bus (See col. 3, lines 28-31), a grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) indicating that a device (i.e., node) in control of said link bus is transferring information on said link bus, and a grant-other state (i.e., wait phase 48 in Fig.

2) indicating that another device is in control of said link bus (i.e., the current node loses the control of the bus, the another node wins the control of the bus; See col. 2, lines 45-68).

Referring to claim 43, Frame teaches said satellite device (i.e., node 12 in Fig. 1) modifies its internal arbitration state and status information by changing its internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2), and wherein said link hub (i.e., node 16 in Fig. 1) modifies its internal arbitration state and status information by changing its internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 44, Frame teaches said satellite device (i.e., node 12 in Fig. 1) modifies its internal arbitration state and status information by changing its internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2), and wherein said link hub (i.e., node 16 in Fig. 1) modifies its internal arbitration state and status information by changing its internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 45, Frame teaches said internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (e.g., arbitration request from enabled message node 14 and 16 in Fig. 1 via enabled path 42 of Fig. 2, i.e., enabled arbitration status; See col. 3, lines 1-3), bus master transfer in progress (i.e., transfer phase 52 after the node is selected as an arbitration winner), bus slave arbitration request (e.g., path 44 of Fig. 2 for disabled message node 12 in Fig. 1, i.e., disabled arbitration status; See col. 3, lines 5-8), and bus slave transfer in progress (i.e., wait phase 48 after the node is lost the bus control; a data transfer on the bus is controlled by another node).

Referring to claim 46, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus master arbitration request (i.e., an arbitration request at t_2 after transfer completion at t_1) and not said bus slave arbitration request (i.e., not an arbitration request at t_1 from enabled message

nodes). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said park state to said grant-other state if said internal status reflects said bus master arbitration request and not said bus slave arbitration request.

Referring to claim 47, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes, and the highest priority node wins to control the bus; See col. 3, lines 42-45).

Referring to claim 48, Frame teaches said internal arbitration state is changed from said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes) and not said bus slave transfer in progress state (i.e., after completion the bus slave transfer in progress state, caused by a selected arbitration request at t_1 and transfer phase at t_1). Refer to col. 3, lines 45-47.

Referring to claim 49, Frame teaches said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., an arbitration request at t_1 from enabled message nodes, which has been waiting in wait phase 48 in Fig. 2) and not said bus master transfer in progress state (i.e., after completion the transfer phase at t_2, caused by a reselected arbitration request at t_2 after transfer completion at t_1). See Fig. 2 and col. 3, lines 21+ for the operation of the fair arbitration scheme.

Referring to claim 50, Frame teaches said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said park state (i.e., bus idle state 40 in Fig. 2) if said internal status does not reflect said bus master arbitration request (i.e.,

no arbitration request at t_2 after transfer completion at t_1), said bus slave arbitration request (i.e., no arbitration request at t_1 from enabled message nodes) and said bus master transfer in progress state (i.e., no reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if said internal status does not reflect said bus master arbitration request, said bus slave arbitration request and said bus master transfer in progress state, i.e., said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if the bus is not busy.

7. Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic [US 6,516,375 B1] as applied to claims 1, 2, 16-20, 34, 35, 38, 40, 51, 52, 55 and 56 above, and further in view of Singh et al. [US 6,609,171 B1; hereinafter Singh].

Referring to claims 53 and 54, Ajanovic discloses all the limitations of the claims 53 and 54, respectively, except that does not teach said link bus is one of a quad pumped source strobed bus and a double pumped source strobed bus.

Singh discloses a multi-pumped signaling mode operation (See col. 6, lines 33+), wherein a link bus (i.e., processor bus 117 in Fig. 2) is one of a quad pumped source strobed bus (See col. 6, lines 43+) and a double pumped source strobed bus (See col. 11, lines 14+) according to a multi-pumped signaling mode (See col. 6, lines 33+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said means for signaling multi-pumped bus (e.g., strobe generator, strobe signal lines, and multi-pumped signaling mode controller), as disclosed by Singh, on said link bus and its connected devices (i.e., bus adapter and module), as disclosed by Ajanovic, for the advantage of

increasing bus throughput by operating said link bus in the multi-pumped signaling mode (See Singh, col. 2, lines 39-42).

Response to Arguments

8. Applicant's arguments filed on 27th of December 2004 with respect to claims 1, 19, 34 and 51 have been considered but are moot in view of the new grounds of rejection.

In response to the Applicant's note, see the Response page 19, lines 5-7, with respect to the rejection based on 35 U.S.C. §102(e) and §103(a), the Office Action erroneously refers to the Ajanovic patent as U.S. Patent No. 6,539,444 instead of U.S. Patent No. 6,516,375, has been fully considered and the Examiner notices that there was a typographical error, such that erroneous referring to the Ajanovic as U.S. Patent No. 6,539,444 instead of U.S. Patent No. 6,516,375. However, the Office Action clearly shows that all the claim rejections under 35 U.S.C. §102(e) and §103(a) are unpatentable over Ajanovic, Frame, and/or Singh. Thus, this erroneous referring to Ajanovic as US 6,539,444 did not affect the ground of claim rejections.

In response to the Applicant's arguments with respect to the newly amended limitations, such that "a link bus comprising a link bus hub and a plurality of link bus segments, each link bus segment comprising a plurality of lines for communicating commands, addresses, data, and a single-bit link status signal, each link bus segment coupled to said link bus hub and one respective satellite device to form a point-to-point link between said link bus hub and respective satellite device one of said respective satellite device" in the exemplary claim 1, the Examiner believes that Ajanovic reference in the record still suggests the amended limitations (See paragraph 4 of the instant Office Action, claims 1, 2, 16-20, 34, 35, 38, 40, 51, 52, 55 and 56 rejection under 35 U.S.C. 102(e) as being anticipated by Ajanovic).
Thus, the Applicant's arguments on this point are moot in view of the new grounds of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee

Examiner
Art Unit 2112

cel/

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